Notice of Allowability	Application No.	Applicant(s)	
	09/972,404	STEWART ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendments filed 21 December 2004 and 31 March 2005*.

2. ☒ The allowed claim(s) is/are *1-18, 19-20, 21, and 22 renumbered as 1-18, 20-21, 19, and 22 respectively*.

3. ☒ The drawings filed on *21 December 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. The attached is a substitute copy of the claims. The copy of the Amendment filed on 31 March 2005 in response to a Notice of Non-compliance sent by the office on 16 March 2005 entered was not clear on which text had been struck through, i.e. must be deleted, and which text had been underlined, i.e. must be added. The attached substitute copy is a clearer copy of the amended claims so that there is no question on which text to delete and which text to add. No amendments have been made by the Examiner.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

4. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
9 June 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently Amended) A system containing an N-word sequence of single-word and double-word instructions and an instruction decoder, wherein the double-word instructions comprise a marker bit pattern, and wherein the instruction decoder comprises logic for implementing a binary decision tree ~~representing every combination of single-word and double-word instructions possible for the N-word sequence and identifying each marker bit pattern combination that corresponds to a unique combination of single-word and double-word instructions~~having a set of nodes arranged from a top-most node to a bottom-most node representing successively preceding memory address locations relative to an address location requested by a microprocessor, and wherein the logic is configured by the binary decision tree to determine if an instruction corresponding to an address location immediately preceding the address location requested by the microprocessor is a single-word instruction or a double-word instruction depending on whether tests performed on at least two nodes lower than the top-most node determines that the instructions corresponding to at least two successively preceding memory address locations contain the marker bit pattern.

2. (Currently Amended) The system as recited in claim 1, ~~further comprising a microprocessor, such that~~ wherein the instruction decoder is contained within the microprocessor and such that ~~each~~ a unique combination of single-word and double-word instructions in the N-word sequence is executable by the microprocessor.

3. (Currently Amended) The system as recited in claim ~~2~~1, further comprising a memory and a cache, wherein the N-word instruction sequence is transferred from the memory to the cache in response to the microprocessor requesting a specific single-word or double-word instruction present within the N-word sequence.

4. (Currently Amended) The system as recited in claim ~~3~~1, wherein each word in the N-word sequence corresponds to one of a series of N consecutive memory addresses.

5. (Currently Amended) The system as recited in claim [[4]]1, wherein the instruction decoder is further adapted to identify the corresponding address of at least one single-word or double-word instruction within each unique combination of single-word and double-word instructions in the N-word sequence.

6. (Currently Amended) The system as recited in claim [[4]]1, wherein the instruction decoder is further adapted to identify the corresponding address of at least one single-word or double-word instruction within a unique combination of single-word and double-word instructions having addresses prior to that of the instruction requested by the microprocessor.

7. (Original) The system as recited in claim 2, wherein the microprocessor further comprises a pipeline, into which single-word and double-word instructions from the N-word sequence pass in order to be executed by the microprocessor.

8. (Original) The system as recited in claim 1, wherein the marker bit pattern is part of the op code of each double-word instruction.

9. (Original) The system as recited in claim 1, wherein the instruction decoder is implemented using standard logic cells, and shares a common semiconductor substrate with the microprocessor within an integrated circuit.

10. (Currently Amended) A method for parsing a sequence of N words into a unique combination of single-word and double-word instructions, comprising:

detecting occurrences of a marker bit pattern present in the op code of each of the double-word instructions and absent from any of the single-word instructions;

creating a binary decision tree to associate with every possible N-word combination of single-word and double-word instructions a corresponding ~~unique combination of~~ marker bit ~~patterns~~pattern; and

employing the binary decision tree to determine ~~the unique combination of single-word and double-word instructions in the sequence of N-words on the basis of the detected occurrences of marker bit patterns~~ whether an instruction at a top node of the tree

corresponding to a first preceding address location immediately preceding an address location requested by a microprocessor is a single-word or double-word instruction depending on whether at least two instructions below the top node of the tree corresponding to successive address locations immediately preceding the first preceding address location contains the marker bit pattern.

11. (Currently Amended) The method as recited in claim 10, further comprising employing an instruction decoder within a the microprocessor to parse the sequence of N words into a unique combination of single-word and double-word instructions, wherein the microprocessor is adapted to execute said single-word and double-word instructions.

12. (Original) The method as recited in claim 11, further comprising transferring the sequence of N words from a memory to a cache in response to the microprocessor requesting a specific single-word or double-word instruction present within the sequence of N words.

13. (Original) The method as recited in claim 12, wherein each word in the sequence of N words corresponds to one of N consecutive memory addresses.

14. (Original) The method as recited in claim 13, further comprising identifying the corresponding address of at least one single-word or double-word instruction within each unique combination of single-word and double-word instructions present within the sequence of N words.

15. (Original) The method as recited in claim 14, further comprising identifying the corresponding address of at least one single-word or double-word instruction within a unique combination of single-word and double-word instructions present within the sequence of N words and having addresses prior to that of the instruction requested by the microprocessor.

16. (Original) The method as recited in claim 14, further comprising, after parsing the sequence of N words into a unique combination of single-word and double-word instructions, placing said single-word and double-word instructions into a pipeline in order to be executed by the microprocessor.

17. (Original) The method as recited in claim 10, further comprising including the marker bit pattern within the op code of all double-word instructions and omitting it from all single-word instructions.

18. (Original) The method as recited in claim 10, further comprising implementing the binary decision tree and marker bit pattern detection using standard logic within the microprocessor.

19. (Currently Amended) A memory medium, comprising:

an N-word sequence of single-word and double-word instructions, wherein the op-code of the double-word instructions contain a marker bit pattern;

a binary decision tree, representing every possible combination of occurrences of the marker bit pattern for the N-word sequence, and identifying each combination associated with a unique sequence of single-word and double-word instructions; and

means for consulting the binary decision tree to determine ~~a unique sequence of single-word and double-word instructions based on the particular combination of occurrences of the marker bit pattern in the N-word sequence~~ whether an instruction at a top node of the tree corresponding to a first preceding address location immediately preceding an address location requested by a microprocessor is a single-word or double word instruction depending on whether at least two instructions below the top node of the tree corresponding to successive address locations immediately preceding the first preceding address location contains the marker bit pattern.

20. (Original) The memory medium as recited in claim 19, wherein the N-word sequence of single-word and double-word instructions is contained within a memory coupled to a microprocessor and the binary decision tree is implemented by logic elements within the microprocessor, and wherein the microprocessor and memory occupy a monolithic substrate.

21. (New) The method as recited in claim 10, further comprising determining whether an instruction at a first node immediately beneath the top node of the tree corresponding to a second preceding address location immediately preceding the first preceding address is a single-word or double-word instruction depending on whether at least two instructions below the first node of the tree corresponding to successive address locations immediately preceding the second preceding address location contains the marker bit pattern.

22. (New) The memory medium as recited in claim 19, further comprising consulting the binary decision tree to determine whether an instruction at a first node immediately beneath the top node of the tree corresponding to a second preceding address location immediately preceding the first preceding address is a single-word or double-word instruction depending on whether at least two instructions below the first node of the tree corresponding to successive address locations immediately preceding the second preceding address location contains the marker bit pattern.

Amendments to the Drawings

Attached are replacement sheets for Figs. 1-11. Amendments have been made only to Figs. 1-4 to indicate them as "Prior Art." No further changes have been made to the drawings. Approval of the amended drawings is respectfully requested.

Attachment: Replacement sheets, Figs. 1-11.

Accepted
AL
6-8-2005